CLAIMS

1. A method of transferring read data from a memory device, the memory device including a data bus and including at least one data masking pin adapted to receive a data masking signal during write operations of the memory, the method comprising:

placing a current read data word on the data bus, the read data word including a plurality of data signals and each data signal having a logic state;

developing a next read data word, the next read data word including a plurality of data signals and each data signal having a logic state;

comparing the logic state of each data signal in the current read data word to the logic state of the corresponding data signal in the next read data word;

determining the number of data signals in the next read data word that are changing from a first logic state in the current read data word to the complementary logic state in the next read data word;

when the determined number of data signals changing from the first logic state to the complementary logic state is greater than N,

developing an inverted next read data word, each data signal in the inverted next read data word having a logic state that is the complementary logic state of the corresponding data signal in the next read data word, and

activating a data bus inversion signal;

placing the inverted next read data word on the data bus; and

applying the activated data bus inversion signal on one of the data masking pins.

2. The method of claim 1 wherein each data word includes 2N data signals.

3. The method of claim 2 wherein the data bus includes X data signals, X being an integer multiple of 2N, and wherein a plurality of inverted next read data words are simultaneously applied on the data bus, each inverted next data word having an associated data bus inversion signal applied on an associated data masking pin.

4. The method of claim 1 further comprising deactivating the data bus inversion signal when the determined number of data signals changing from the first logic state to the complementary logic state is less than or equal to N.

5. A method of transferring read data from a memory device, the memory device including a data bus and including a data masking pin adapted to receive a masking signal during write operations of the memory device, the method comprising:

placing a sequence of read data words on the data bus; and

applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted.

6. The method of claim 5 wherein the data bus inversion signal corresponds to a sequence of bits, each bit indicating whether a corresponding read data word in the sequence is to be inverted or not be inverted, and the bit associated with a particular read data word is applied on the data masking pin coincident with the particular read data word being placed on the data bus.

7. The method of claim 5 wherein each read data word includes a plurality of data bits, and wherein applying a data bus inversion signal on the data masking pin comprises:

comparing the logic state of each data bit in a current read data word being placed on the data bus to the logic state of a corresponding data bit in a next read data word in the sequence that is to be placed on the data bus;

determining the number of data bits in the next read data word that are changing from a first logic state in the current read data word to the complementary logic state in the next read data word;

when the determined number of data bits changing from the first logic state to the complementary logic state is greater than N,

developing an inverted next read data word, each data signal in the inverted next read data word having a logic state that is the complementary logic state of the corresponding data signal in the next read data word;

activating the data bus inversion signal; and

placing the inverted next read data word on the data bus and the activated data bus inversion signal on the data masking pin; and

when the determined number of data bits changing from the first logic state to the complementary logic state is less than or equal to N,

deactivating the data bus inversion signal; and

placing the next read data word on the data bus and the deactivated data bus inversion signal on the data masking pin.

8. The method of claim 5 wherein the memory device includes a plurality of data masking pins, each read data word comprises 2N data bits, and the data bus includes X data bits where X is an integer multiple of 2N, and wherein a plurality of next read data words are simultaneously applied on the data bus, each next data word having an associated data bus inversion signal applied on an associated data masking pin.

9. A method of transferring data over a data bus, the method comprising:

generating a sequence of data words, at least one data word including data bus inversion data;

applying the sequence of data words on the data bus;

storing the sequence of data words; and

applying the data bus inversion data to invert or not invert the data contained in the stored data words.

10. The method of claim 9 wherein generating a sequence of data words comprises:

accessing N data words, each data word including M bits;

comparing groups of bits in each pair of consecutive data words to determine for each group the number of bits changing from a first logic state in the first word in the pair to the complementary logic state in the second word in the pair;

generating a plurality of data bus inversion bits in response to the comparing of groups of bits; and

generating at least one data bus inversion word including the data bus inversion bits;

selectively inverting or not inverting the bits in the N data words in response to the generated data bus inversion bits; and

forming the sequence of data words including the N data words having the selectively inverted or not inverted bits and the data bus inversion word.

11. The method of claim 10 further comprising:

comparing groups of bits in the generated data bus inversion word and the first data word in the sequence to determine the number of bits changing from a first logic state in the data bus inversion word to the complementary logic state in the first data word in the sequence;

generating a final data bus inversion bit in response to each compared group; and

placing each final data bus inversion bit in the data bus inversion word.

12. The method of claim 11 wherein generating a final data bus inversion bit in response to each compared group comprises selecting a value for the final data bus inversion bit associated with one of the groups.

13. The method of claim 10 wherein N equals 8 and M equals 32, and wherein each group of bits comprises 8 bits.

14. The method of claim 9 wherein one data word in the sequence includes the data bus inversion data.

15. The method of claim 9 wherein all data words in the sequence are stored prior to applying the data bus inversion data to invert or not invert the data contained in the stored data words.

16. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a data masking terminal adapted to receive a data masking signal during write operations of the memory device; and

a read/write circuit coupled to the data bus, memory-cell array, and the data masking terminal, the read/write circuit operable during read operations to compare the number of bits changing from a first logic state in a current read data word on the data bus to the complementary logic state in a next read data word received from the memory-cell array, and operable in a first mode when the number of bits changing state is greater than a threshold value to apply an inverted next read data word on the data bus and apply an active a data bus inversion signal on the data masking terminal, and operable in a second mode when the number of bits changing state is less than or equal to the threshold value to apply the next read data word on the data bus and apply an inactive data bus inversion signal on the data masking terminal.

17. The memory device of claim 16 wherein the memory device comprises a DDR SDRAM.

18. The memory device of claim 16 further comprising a plurality of data masking terminals and the read/write circuit operable to compare groups of bits in the current and next read data words, and to develop a corresponding data bus inversion signal for each group and apply each data bus inversion signal on a respective data masking terminal.

19. The memory device of claim 16 wherein the read/write circuit comprises:

a storage circuit coupled to the memory-cell array to receive a true read data word including a plurality of bits, and the storage circuit operable to store each true read data word responsive to a clock signal;

an inversion circuit coupled to the storage circuit to receive the stored true read data word and operable responsive to an inversion control signal being active to invert the bits in the stored read data word to generate an inverted read data word and apply the inverted read data word on an output, and operable responsive to the inversion control signal being inactive to apply the true read data word on the output;

a data driver circuit coupled to the output of the inversion circuit and to the data bus, and operable to apply the read data word from the inversion circuit on the data bus responsive to a clocks signal; and

a comparison circuit coupled to the storage circuit to receive the true read data word and to the data bus to receive the current read data word, and operable to determine the number of bits changing from the first logic state to the complementary logic state and to activate the inversion control signal responsive to the number of bits being greater than the threshold value and deactivate the inversion control signal responsive to the number of bits being less than or equal to the threshold value.

20. A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during read operations to generate a sequence of read data words including at least one data word including data bus inversion data, and operable to apply the sequence of read data words on the data bus.

21. The memory device of claim 20 wherein the read/write circuit is further operable during write operations to store a sequence of write data words received on the data bus and thereafter apply data bus inversion data contained in at least one of the received write data words invert or not invert data contained in the other write data words and transfer the data to the memory-cell array.

22. The memory device of claim 20 wherein the memory device comprises a DDR SDRAM.

23. The memory device of claim 20 wherein the sequence of read data words comprises 9 read data words, one of the read data words including the data bus inversion data.

24. The memory device of claim 23 wherein each read data word includes 32 bits, and each of the 32 bits in the data word including the data bus inversion data applies to a corresponding byte in one of the 8 other read data words.

25. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit;

a data masking terminal adapted to receive a data masking signal during write operations of the memory device; and

a read/write circuit coupled to the data bus, memory-cell array, and the data masking terminal, the read/write circuit operable during read operations to compare the number of bits changing from a first logic state in a current read data word on the data bus to the complementary logic state in a next read data word received from the memory-cell array, and operable in a first mode when the number of bits changing state is greater than a threshold value to apply an inverted next read data word on the data bus and apply an active a data bus inversion signal on the data masking terminal, and operable in a second mode when the number of bits changing state is less than or equal to the threshold value to apply the next read data word on the data bus and apply an inactive data bus inversion signal on the data masking terminal.

26. The computer system of claim 25 wherein the memory device comprises a DDR SDRAM.

27. The computer system of claim 25 further comprising a plurality of data masking terminals and the read/write circuit operable to compare groups of bits in the current and next read data words, and to develop a corresponding data bus inversion signal for each group and apply each data bus inversion signal on a respective data masking terminal.

28. The computer system of claim 25 wherein the read/write circuit comprises:

a storage circuit coupled to the memory-cell array to receive a true read data word including a plurality of bits, and the storage circuit operable to store each true read data word responsive to a clock signal;

an inversion circuit coupled to the storage circuit to receive the stored true read data word and operable responsive to an inversion control signal being active to invert the bits in the stored read data word to generate an inverted read data word and apply the inverted read data word on an output, and operable responsive to the inversion control signal being inactive to apply the true read data word on the output;

a data driver circuit coupled to the output of the inversion circuit and to the data bus, and operable to apply the read data word from the inversion circuit on the data bus responsive to a clocks signal; and

a comparison circuit coupled to the storage circuit to receive the true read data word and to the data bus to receive the current read data word, and operable to determine the number of bits changing from the first logic state to the complementary logic state and to activate the inversion control signal responsive to the number of bits being greater than the threshold value and deactivate the inversion control signal responsive to the number of bits being less than or equal to the threshold value.

29. A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a read/write circuit coupled to the data bus and the memory-cell array, the read/write circuit operable during read operations to generate a sequence of read data words including at least one data word including data bus inversion data, and operable to apply the sequence of read data words on the data bus.

30. The computer system of claim 29 wherein the read/write circuit is further operable during write operations to store a sequence of write data words received on the data bus and thereafter apply data bus inversion data contained in at least one of the received write data words invert or not invert data contained in the other write data words and transfer the data to the memory-cell array.

31. The computer system of claim 29 wherein the memory device comprises a DDR SDRAM.

32. The computer system of claim 29 wherein the sequence of read data words comprises 9 read data words, one of the read data words including the data bus inversion data.

33. The computer system of claim 32 wherein each read data word includes 32 bits, and each of the 32 bits in the data word including the data bus inversion data applies to a corresponding byte in one of the 8 other read data words.